US009064904B2

(12) **United States Patent**
Kuo

(10) **Patent No.: US 9,064,904 B2**
(45) **Date of Patent: Jun. 23, 2015**

(54) **MOS P-N JUNCTION SCHOTTKY DIODE DEVICE AND METHOD FOR MANUFACTURING THE SAME**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/308,929**

(22) Filed: **Jun. 19, 2014**

(65) **Prior Publication Data**

US 2014/0295628 A1 Oct. 2, 2014

Related U.S. Application Data

(62) Division of application No. 12/427,256, filed on Apr. 21, 2009, now Pat. No. 8,796,808.

(30) **Foreign Application Priority Data**

Apr. 22, 2008 (TW) ..... 97114729 A

(51) **Int. Cl.**

H01L 21/28	(2006.01)
H01L 21/44	(2006.01)
H01L 29/66	(2006.01)
H01L 29/739	(2006.01)
H01L 29/872	(2006.01)
H01L 29/06	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/66848*** (2013.01); *H01L 29/0619* (2013.01); *H01L 29/0684* (2013.01); ***H01L 29/66143*** (2013.01); ***H01L 29/66356*** (2013.01); ***H01L 29/7391*** (2013.01); ***H01L 29/872*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 29/872; H01L 29/66143; H01L 29/66863; H01L 21/28587
USPC 438/570, 571, 575; 257/471
See application file for complete search history.

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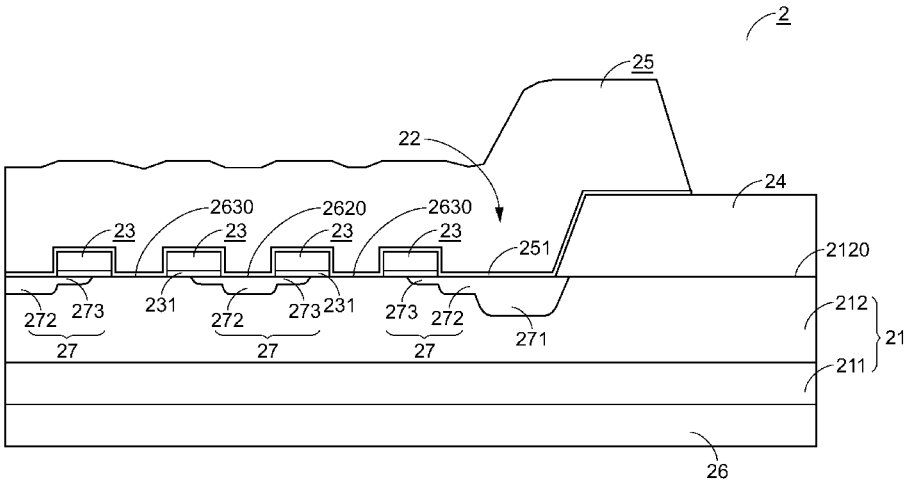
(57) **ABSTRACT**

A MOS P-N junction Schottky diode device includes a substrate having a first conductivity type, a field oxide structure defining a trench structure, a gate structure formed in the trench structure and a doped region having a second conductivity type adjacent to the gate structure in the substrate. An ohmic contact and a Schottky contact are formed at different sides of the gate structure. The method for manufacturing such diode device includes several ion-implanting steps to form several doped sub-regions with different implantation depths to constitute the doped regions. The formed MOS P-N junction Schottky diode device has low forward voltage drop, low reverse leakage current, fast reverse recovery time and high reverse voltage tolerance.

12 Claims, 7 Drawing Sheets



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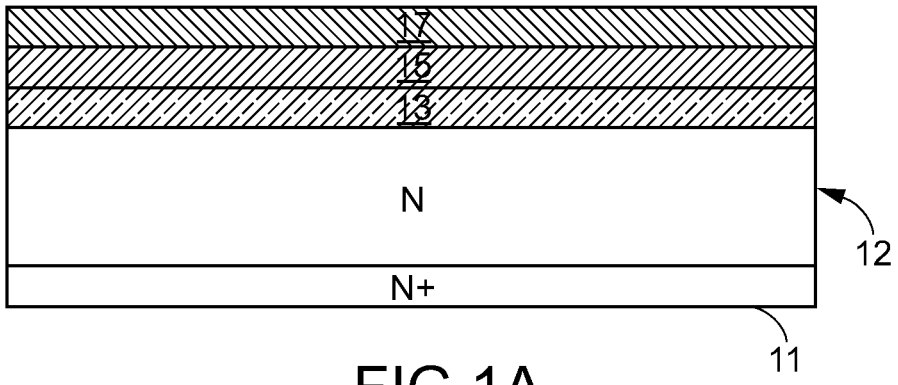


FIG.1A
PRIOR ART

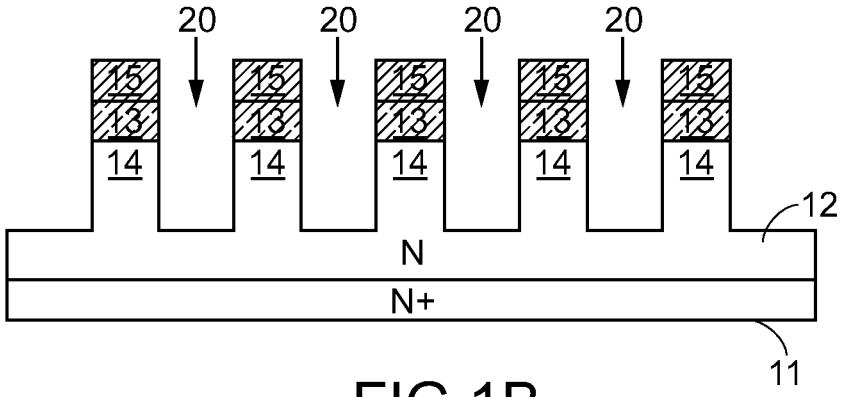


FIG.1B
PRIOR ART

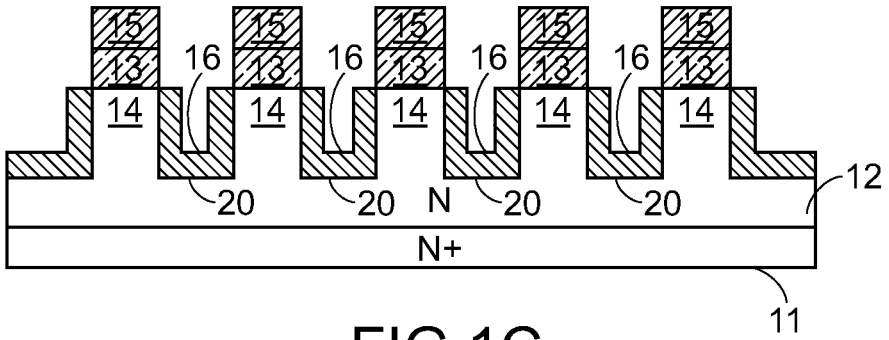


FIG.1C
PRIOR ART

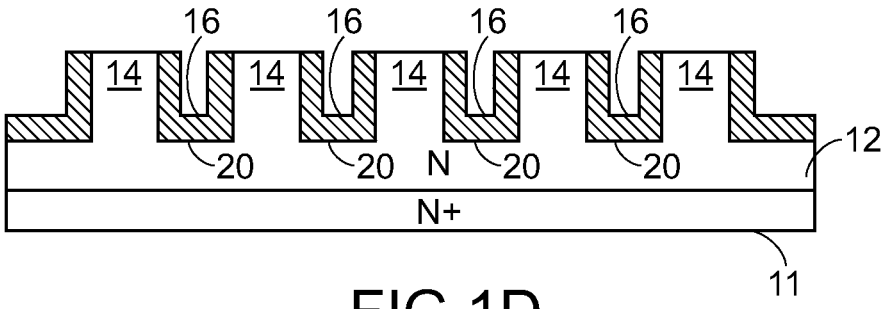


FIG.1D
PRIOR ART

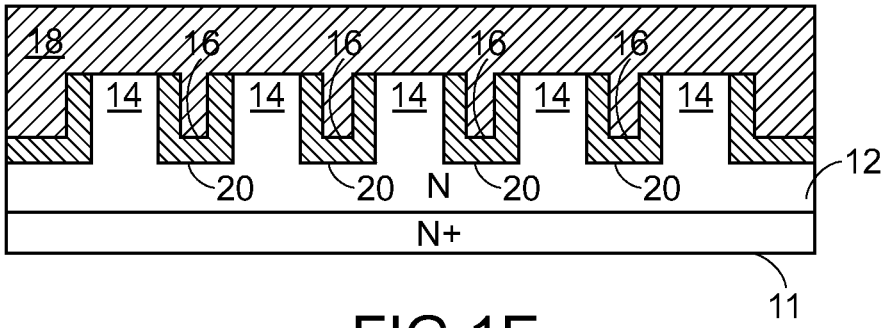


FIG.1E
PRIOR ART

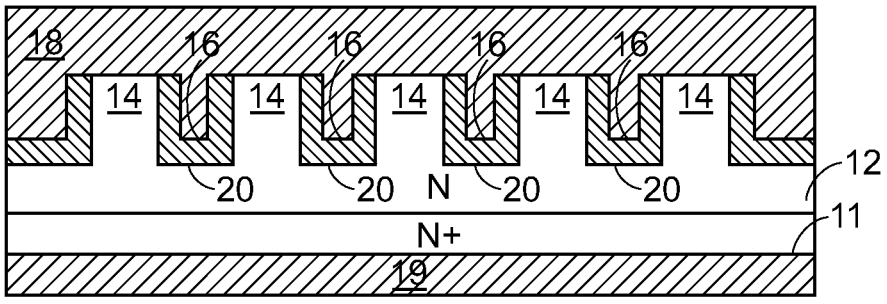
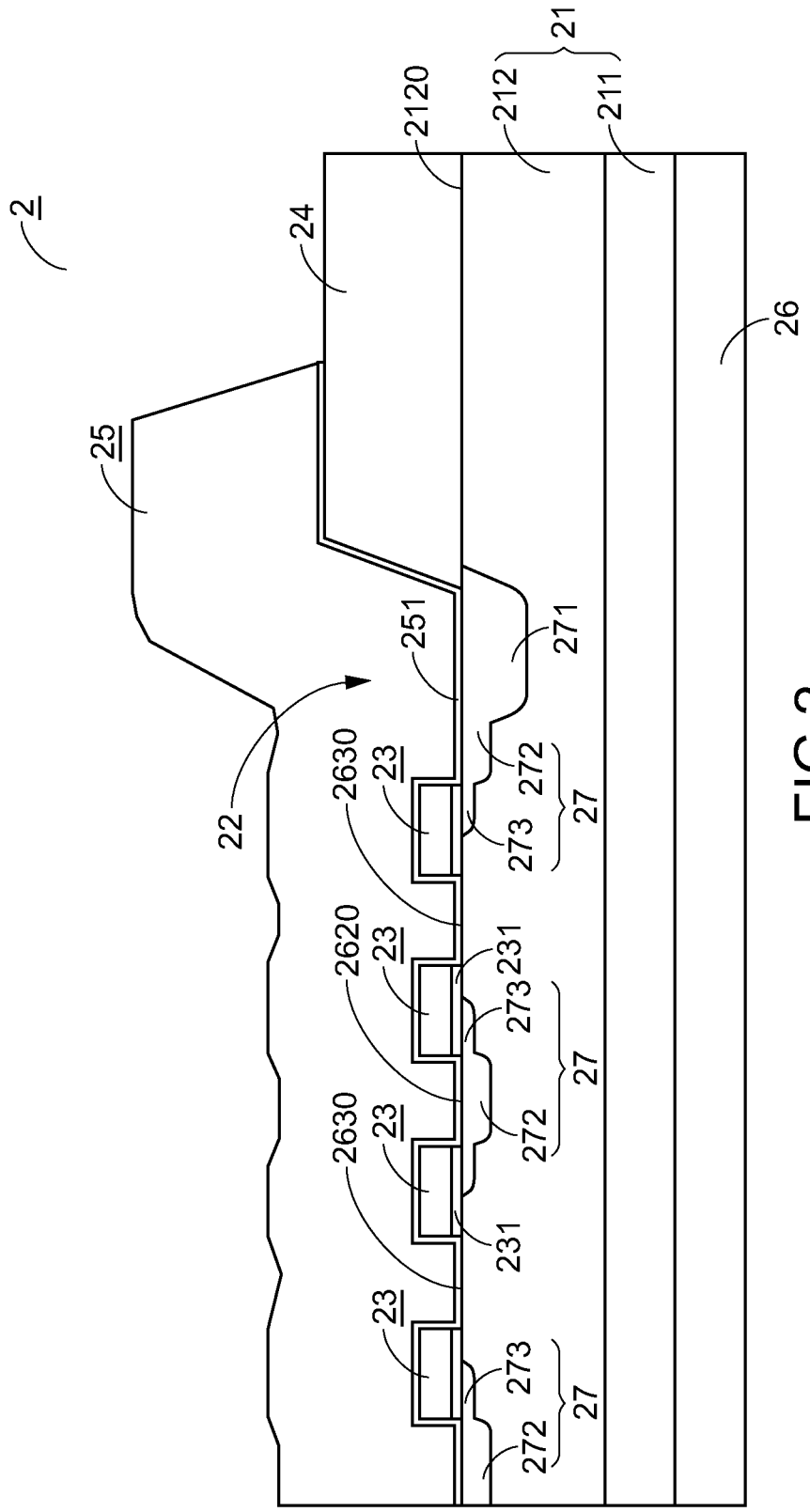


FIG.1F
PRIOR ART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24
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211
21
26
25
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271
22
2630
23
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273
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27
2630
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231
23
273
272
27

FIG.2

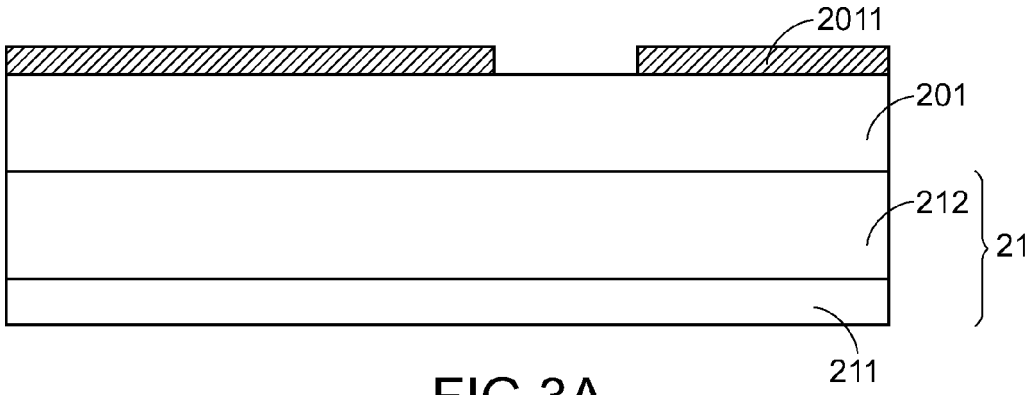


FIG.3A

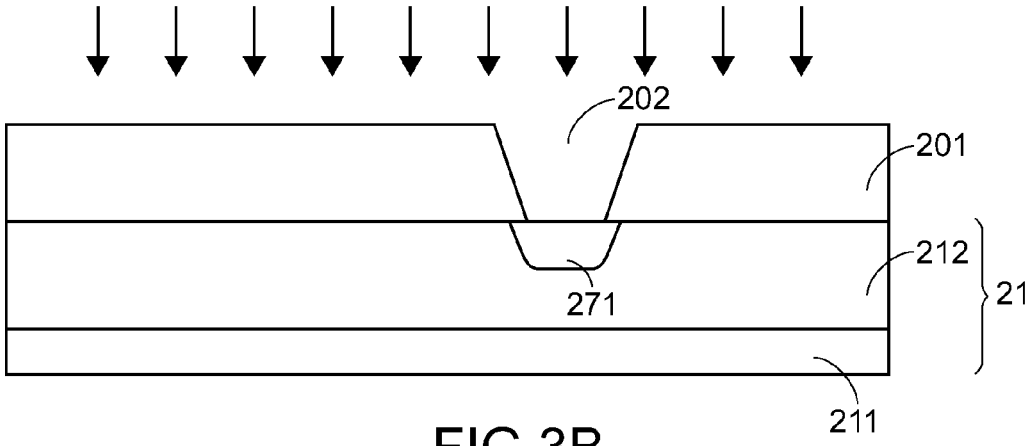


FIG.3B

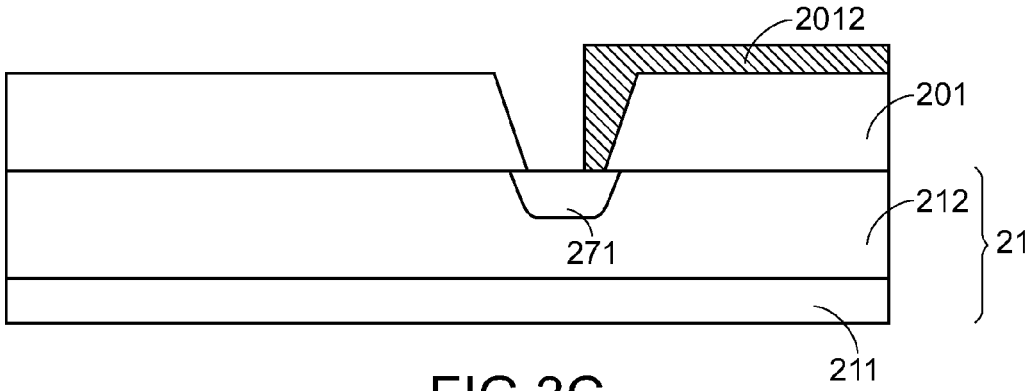


FIG.3C

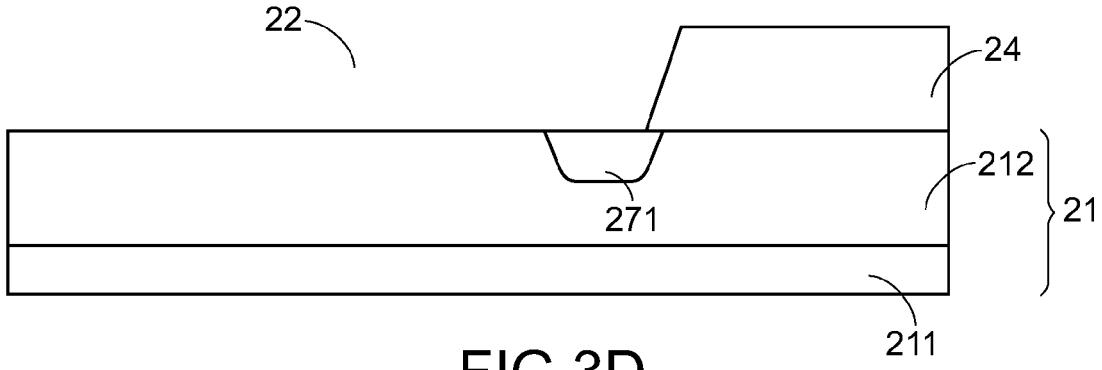


FIG.3D

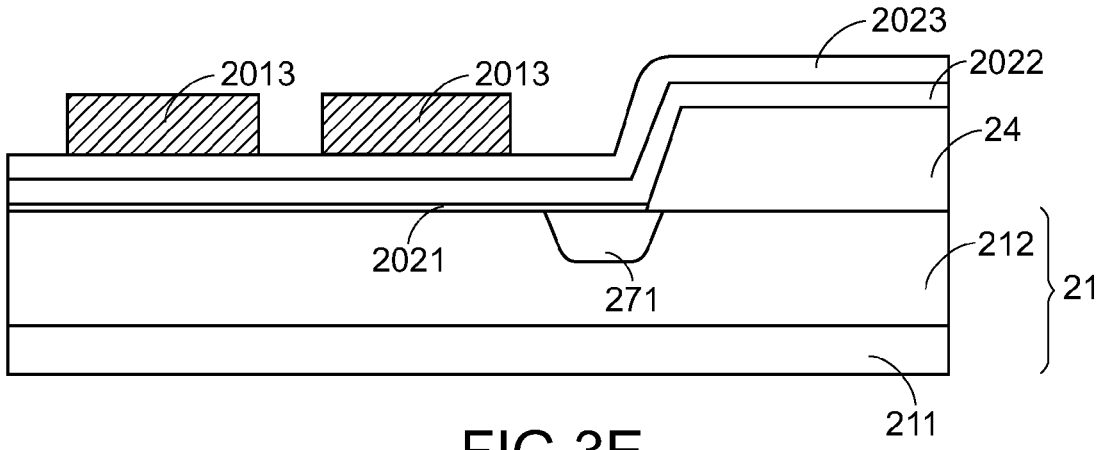


FIG.3E

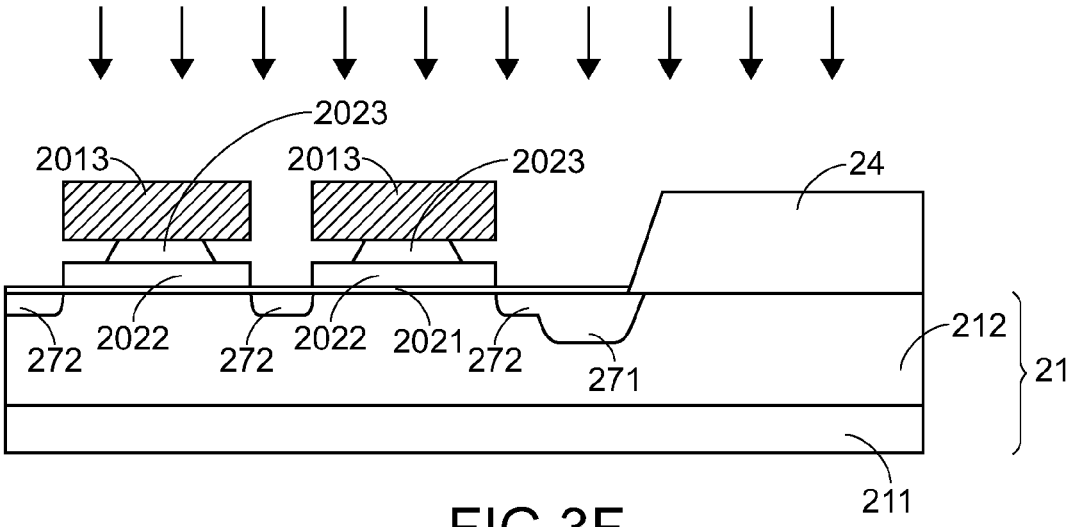
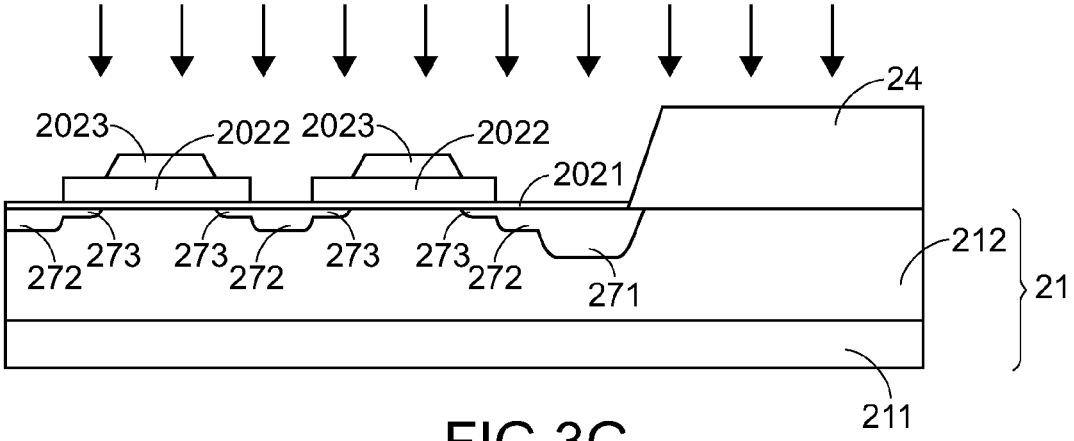

2023
2013
2013
2023
24
272
2022
272
2022
2021
272
271
212
21
211

FIG.3F


24
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2021
272
273
273
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273
272
271
212
21
211

FIG.3G

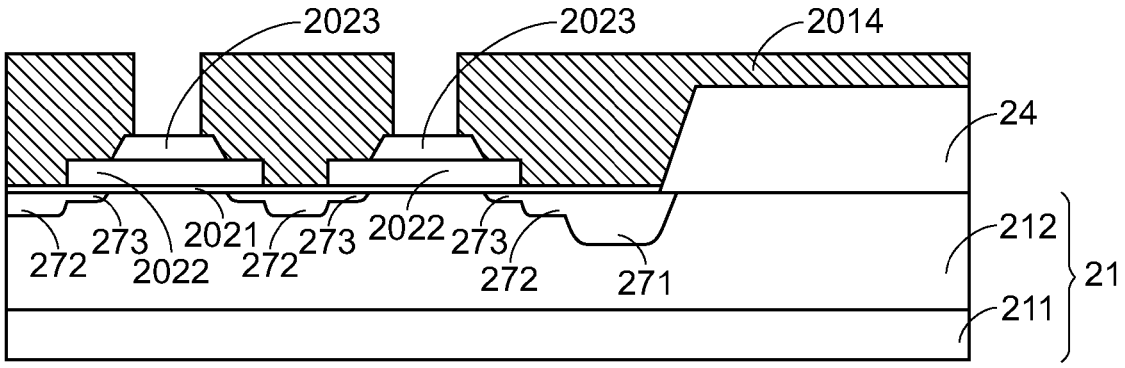

FIG.3H

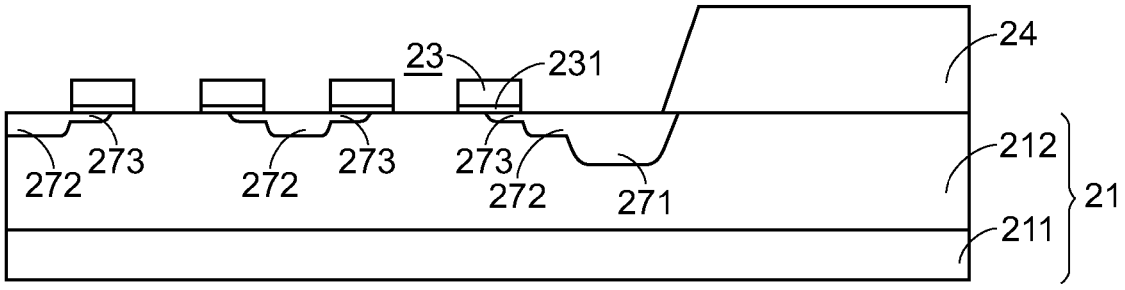

FIG.3I

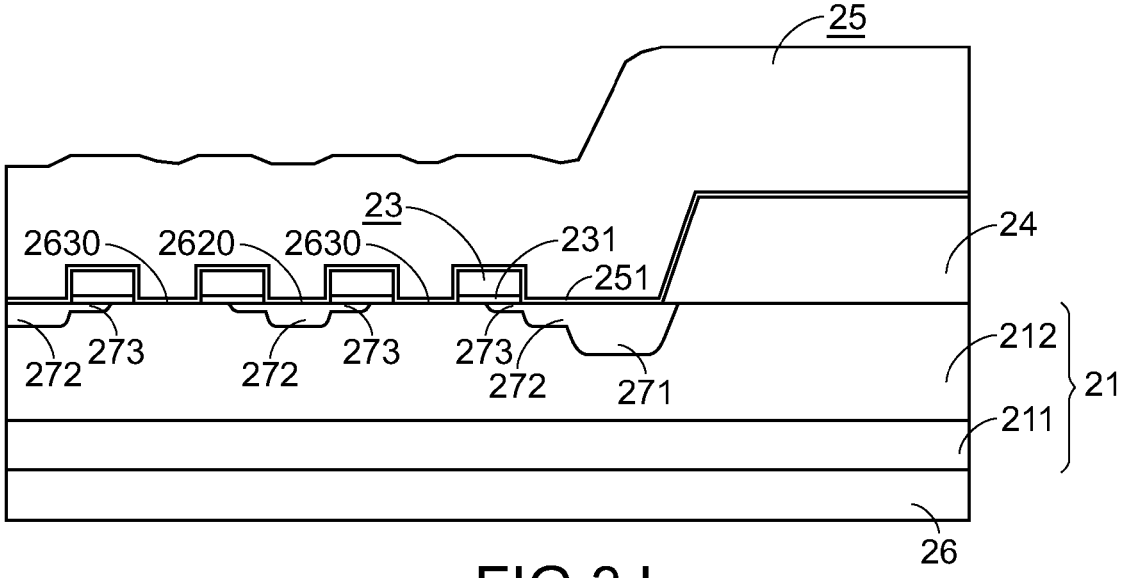

FIG.3J

MOS P-N JUNCTION SCHOTTKY DIODE DEVICE AND METHOD FOR MANUFACTURING THE SAME

This is a divisional application of co-pending U.S. Ser. No. 12/427,256, filed Apr. 21, 2009, which claims the benefit of Taiwan application Serial No. 97114729, filed Apr. 22, 2008, the subject matter of which is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to a metal-oxide-semiconductor (MOS) P-N junction Schottky diode device and a method for manufacturing the diode device, and more particularly to a MOS P-N junction Schottky diode device with low leakage current, low forward voltage drop, high reverse voltage and fast reverse recovery time.

BACKGROUND OF THE INVENTION

A Schottky diode is a unipolar device using electrons as carriers, which is characterized by high switching speed and low forward voltage drop. Hence, Schottky diodes are used in many applications. The limitations of Schottky diodes are the relatively low reverse voltage tolerance and the relatively high reverse leakage current. The limitations are related to the Schottky barrier determined by the metal work function of the metal electrode, the band gap of the intrinsic semiconductor, the type and concentration of dopants in the semiconductor layer, and other factors. In contrast to the Schottky diode, a P-N junction diode is a bipolar device that can pass more current than the Schottky diode. However, the P-N junction diode has a forward voltage drop higher than that of the Schottky diode, and takes longer reverse recovery time due to a slow and random recombination of electrons and holes during the recovery period.

A typical device of Schottky diode device with MOS trench has been disclosed by U.S. Pat. No. 5,365,102. Please refer to FIGS. **1A-1F** illustrating the manufacturing method of forming the trench MOS barrier Schottky rectifier (TMBSR). Firstly, a substrate **11** with an N-type epitaxial layer **12** grown thereon is provided. Then, a multilayered stack of a pad oxide layer **13**, a mask nitride layer **15** and a photo-resist layer **17** is formed on the N-type epitaxial layer **12**. The pad oxide layer **13** may relieve interlayer stress between the N-type epitaxial layer **12** and the mask nitride layer **15** (FIG. **1A**). A photolithography and etching step is performed to partially remove the mask nitride layer **15**, the pad oxide layer **13** and the N-type epitaxial layer **12** so as to form discrete mesas **14** and trenches **20** defined between the mesas **14** (FIG. **1B**). A thermal oxide layer **16** is then formed on the trench bottoms and trench sidewalls (FIG. **1C**). After the remaining portions of the mask nitride layer **15** and the pad oxide layer **13** are removed (FIG. **1D**), an anode metal layer **18** is subsequently plated thereon (FIG. **1E**). The anode metal layer **18** is then subjected to a metal patterning step, wherein a Schottky barrier contact is formed on the interface between the anode metal layer **18** and the mesa **14** of the N-type epitaxial layer **12**. At last, a backside grinding step is conducted on the backside of the wafer and a cathode electrode **19** is formed thereon (FIG. **1F**). The process of manufacturing the TMBSR is thus basically completed.

The TMBSR made by the aforementioned method has a low forward voltage drop but a high reverse leakage current. If a lower reverse-biased leakage current is desired, one solution is to choose a metal electrode with a higher work function to reduce the reverse leakage current. However, in this context the forward voltage drop of the TMBSR is increased. Accordingly, there is a trade-off between the forward voltage drop and the reverse leakage current.

An alternative way in reducing the reverse leakage current is to deepen the trenches so as to increase the length of the pitch-off channel to inhibit the reverse leakage current. Nevertheless, such device cannot resist high reverse voltage, unless the thickness of the N-type epitaxial layer **12** is increased to improve the reverse voltage tolerance. In conclusion, Schottky diode is not suitable for high power application. Current commercial Schottky diode device has a reverse voltage tolerance less than 600 V. In fact, so-called 600 V Schottky diode device consists of two TMBSRs connected in series and each has a reverse voltage tolerance of 300 V, which leads to a higher forward voltage drop. Thus, it is a challenge to design a diode device with high reverse voltage tolerance (e.g. higher than 600 V), low forward voltage drop, low reverse leakage current and fast reverse recovery time. Therefore, there is a need of providing a diode device with these properties to obviate the drawbacks encountered from the prior art. Furthermore, a cost-effective method for manufacturing such diode device is also desired.

SUMMARY OF THE INVENTION

The present invention provides a MOS P-N junction Schottky diode device combining a Schottky diode, an n-channel MOS structure and a P-N junction diode to achieve better performance involving low reverse leakage current, low forward voltage drop, high reverse voltage and fast reverse recovery time.

The present invention also provides a convenient and cost-effective method for manufacturing the MOS P-N junction Schottky diode device. Fewer masks are required for this manufacturing method.

In accordance with an aspect of the present invention, the MOS P-N junction Schottky diode device includes a substrate, a field oxide structure, a gate structure, a doped region, a top electrode and a bottom electrode. The top electrode and the bottom electrode are formed at opposite sides of the substrate. The doped region has different conductivity type from the substrate. Besides, an ohmic contact is formed between the doped region and the top electrode at one side of the gate structure while a Schottky contact is formed between the substrate and the top electrode at the other side of the gate structure. The field oxide structure defines a trench structure in which the gate structure is formed. The doped region has a plurality of adjacent doped sub-regions with different implantation depths and extends from a surface of the substrate. Hence, a MOS structure, a P-N junction diode and a Schottky diode are provided in the diode device.

In accordance with another aspect of the present invention, a first mask layer having an opening, formed by a first photolithography step and an etching step, is formed on a substrate and a first ion-implanting step is performed through the opening to form a guard ring in the substrate. Then, a second photolithography step and an oxide wet etching step are performed and a portion of the first mask layer is removed to form a field oxide structure defining a trench structure. A conductive semiconductor layer, a second mask layer and a photo-resist layer, patterned by a third photolithography step and defining the conductive semiconductor layer, are formed in the trench structure wherein the remaining second mask layer formed by an isotropic etching step is shorter than the patterned photo-resist layer. A second ion-implanting step and a third ion-implanting step are performed by using the

patterned photo-resist layer and the remaining second mask layer as masks, respectively, to form adjacent doped sub-regions with different implantation depths. A fourth photolithography and etching step is formed to remove the second mask layer and partially remove the conductive semiconductor layer to form a gate structure. At last, a top electrode and a bottom electrode are disposed at opposite sides of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, in which:

FIGS. **1**A-**1**F (prior art) schematically illustrate the manufacturing method of forming the known trench MOS barrier Schottky rectifier;

FIG. **2** is a cross-sectional view illustrating a preferred embodiment of a MOS P-N junction Schottky diode device according to the present invention; and

FIGS. **3**A-**3**J schematically illustrate the manufacturing method for forming the MOS P-N junction Schottky diode device of FIG. **2**.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will now be described more specifically with reference to the following embodiments. It is to be noted that the following descriptions of preferred embodiments of this invention are presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

Referring to FIG. **2**, FIG. **2** schematically illustrates a preferred embodiment of a MOS P-N junction Schottky diode device according to the present invention. Please note that the article "a" or "an" may be used for some elements, but the number of the elements is not limited to "one". The amount may vary with different applications. As shown in FIG. **2**, the MOS P-N junction Schottky diode device **2** primarily includes a substrate **21**, a trench structure **22**, a gate structure **23**, a field oxide structure **24**, a top electrode **25**, a bottom electrode **26** and a doped region **27**. The substrate **21** includes a heavily-doped N-type silicon layer **211** and a lightly-doped N-type epitaxial layer **212**. The field oxide structure **24** is formed on the substrate **21** and defines the trench structure **22**. The gate structure **23** is formed in the trench structure **22** on the N-type epitaxial layer **212** wherein a gate oxide layer **231** is interfaced between the gate structure **23** and the substrate **21**. The top electrode **25** covers the trench structure **22**, the gate structure **23** and the field oxide structure **24**, while the bottom electrode **26** is formed on the opposite surface of the substrate **21**. Both the top electrode **25** and the bottom electrode **26** are made of metal material, for example Al, Al alloy or other suitable metal material. An adhesion layer **251** made of Ti or TiN may be provided between the top electrode **25** and the substrate **21** to enhance the bonding of the top electrode **25** to the substrate **21**.

There are two kinds of contacts established at different sides of the gate structure **23**. Ohmic contact **2620** is formed on the interface between the top electrode **25** and the doped region **27**. On the other hand, Schottky contact **2630** is formed on the interface between the top electrode **25** and an undoped portion of the N-type epitaxial layer **212**.

In this embodiment, the doped region **27** includes a first doped sub-region **272** and a second doped sub-region **273** with different implantation depths. The first doped sub-region **272** is deeper than the second doped sub-region **273**. A guard ring **271** may be formed in the edge of the MOS P-N junction Schottky diode device to define the device region. The first doped sub-region **272**, the second doped sub-region **273** and the guard ring **271** are implanted with P-type dopants. Both of the doped sub-regions **272** and **273** extend from the surface **2120** of the lightly-doped N-type epitaxial layer **212**. It means that no other N doped region will be formed between the doped region **27** and the surface **2120** of the lightly-doped N-type epitaxial layer **212**. The p-type doped sub-regions **272** and **273** together with the lightly-doped N-type epitaxial layer **212** provide a P-N junction adjacent to the n-channel MOS structure including the gate structure **23**, the gate oxide layer **231** and the substrate **21**. At the other side of the n-channel MOS structure, the top electrode **25** together with the lightly-doped N-type epitaxial layer **212** provides a Schottky diode.

According to the present invention, the MOS P-N junction Schottky diode device **2** integrates an n-channel MOS structure with a P-N junction diode and a Schottky diode. By virtue of this structure design, when the MOS P-N junction Schottky diode device **2** is forward-biased, the n-channel MOS structure, the P-N junction diode, the Schottky diode are operated as parallel connection. Hence, the MOS P-N junction Schottky diode device **2** keeps the advantages of the Schottky diode such as low forward voltage drop and high switching speed. When the MOS P-N junction Schottky diode device **2** is reverse-biased, a depletion region is formed in the P-N junction diode and almost no net current flows through the junction. With the increasing reverse voltage, the depletion regions at two sides of the Schottky diode extend to pitch off the channel under the Schottky contact **2630** and the n-channel MOS structure to inhibit the leakage current. Hence, the MOS P-N junction Schottky diode device **2** can withstand high reverse voltage and decrease leakage current. Therefore, the MOS P-N junction Schottky diode device **2** has the advantage over Schottky diode in reverse mode. Because of these advantages, the MOS P-N junction Schottky diode device **2** provides much better performance than the conventional Schottky diode and P-N junction diode.

FIGS. **3**A-**3**J illustrate the manufacturing method for forming the MOS P-N junction Schottky diode of FIG. **2** according to the present invention. As shown in FIG. **3**A, a stack structure including a substrate **21**, a mask oxide layer **201** and a first patterned photo-resist layer **2011** is formed. The substrate **21** includes a heavily-doped N-type silicon layer **211** and a lightly-doped N-type epitaxial layer **212**. The mask oxide layer **201** is grown by thermal oxidation or deposited on the substrate **21**.

In FIG. **3**B, the mask oxide layer **201** is subjected to an etching step to partially remove the mask oxide layer **201** to expose a portion of the lightly-doped N-type epitaxial layer **212**. After removing the first patterned photo-resist layer **2011**, a P-type dopant such as B ion or BF_2 is then implanted through the opening **202** of the mask oxide layer **201**. It is noted that the P-type dopant can be implanted before or after the removal of the photo-resist layer **2011**. A thermal drive-in step is introduced to form the deep guard ring **271** which defines the device region in the lightly-doped N-type epitaxial layer **212**.

In FIG. **3**C, a second patterned photo-resist layer **2012** is formed on a portion of the mask oxide layer **201**, which will form the field oxide structure **24** later. Then, an etching procedure is performed to remove the mask oxide layer **201** not covered by the second patterned photo-resist layer **2012**. After removing the second patterned photo-resist layer **2012**,

the remaining mask oxide layer **201** is the field oxide structure **24** defining the trench structure **22** as shown in FIG. **3**D.

In FIG. **3**E, an insulating layer **2021**, a polysilicon layer **2022** and a mask oxide layer **2023** are sequentially formed on the lightly-doped N-type epitaxial layer **212** and the field oxide structure **24**. The insulating layer **2021** is an oxide layer. The polysilicon layer **2022** may be a doped or undoped polysilicon layer deposited by chemical vapor deposition (CVD). The mask oxide layer **2023** is formed by thermal oxidation. Thereafter, a third patterned photo-resist layer **2013** used for defining the polysilicon layer **2022** is formed on the mask oxide layer **2023**.

Then, an isotropic etching step (e.g. wet etching) and an anisotropic etching step (e.g. dry etching) are performed to partially remove the mask oxide layer **2023** and the polysilicon layer **2022**, respectively. FIG. **3**F shows that the remaining mask oxide layer **2023** is shorter than the remaining polysilicon layer **2022**. A P-type dopant is further implanted into the lightly-doped N-type epitaxial layer **212** by using the third patterned photo-resist layer **2013** as a mask. Hence, the first doped sub-region **272** is formed adjacent to the remaining polysilicon layer **2022**.

In FIG. **3**G, the third patterned photo-resist layer **2013** is removed. A P-type dopant is further implanted into the lightly-doped N-type epitaxial layer **212** by using the mask oxide layer **2023** as a mask. Hence, the second doped sub-region **273** is formed under the polysilicon layer **2022** and adjacent to the first doped sub-region **272**. The second doped sub-region **273** is shallower than the first doped sub-region **272**. It is noted that a rapid thermal annealing (RTA) can be employed to activate all implants at this stage. Separate rapid thermal annealing can be preformed after each individual implanting step as an alternative approach.

In FIG. **3**H, the fourth patterned photo-resist layer **2014** is formed on the trench structure **22** and the filed oxide structure **24** while exposing a portion of the mask oxide layer **2023**. Then, an isotropic etching step (e.g. wet etching) and an anisotropic etching step (e.g. dry etching) are performed to entirely remove the mask oxide layer **2023** and partially remove the polysilicon layer **2022**, respectively. The remaining polysilicon layer **2022** is the gate structure **23** as shown in FIG. **3**I. The fourth photo-resist layer **2014** is removed and an oxide wet dipping step is performed to remove the insulating layer **2021** not covered by the gate structure **23**. The remaining insulating layer **2021** is the gate oxide layer **231** for isolating the gate structure **23** from the active region in the substrate **21**.

At last, the top electrode **25** and the bottom electrode **26** are formed at the opposite sides of the resulting structure, as shown in FIG. **3**J. A metal material, for example Al, Al alloy or other suitable metal material, forms the electrodes **25** and **26** by sputtering and sintering. An adhesion layer **251** may be formed prior to the formation of the top electrode **25**. The adhesion layer **251** is deposited by Ti or TiN sputtering and subjected to a rapid thermal nitridation to enhance the bonding effect. After these steps, the MOS P-N junction Schottky diode device **2** is obtained.

According to the present invention, the MOS P-N junction Schottky diode device has low forward voltage drop in the forward mode and has low reverse leakage current and high voltage tolerance in the reverse mode. Furthermore, the fast reverse recovery time of the MOS P-N junction Schottky diode device increases the switching speed thereof. By integrating the MOS structure and the P-N junction diode to the Schottky diode, the present invention can overcome the trade-off between low forward voltage drop and low reverse leakage current. Furthermore, the manufacturing method according to the present invention uses the fewest photo-resist layers to manufacture the MOS P-N junction Schottky diode device. Therefore, the manufacturing method is highly competitive.

While the invention has been described in terms of what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention needs not to be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. A method for fabricating a metal-oxide-semiconductor (MOS) P-N junction Schottky diode device, comprising steps of:

providing a substrate having a first conductivity type;

forming a field oxide structure defining a trench structure on the substrate;

sequentially forming a conductive semiconductor layer, a first mask layer and a first patterned photo-resist layer defining the conductive semiconductor layer in the trench structure;

performing an isotropic etching step on the first mask layer by using the first patterned photo-resist layer as a mask to have the remaining first mask layer shorter than the first patterned photo-resist layer;

doping the substrate with ions having a second conductivity type using the first patterned photo-resist layer as a mask to form a first doped sub-region in the substrate;

removing the first patterned photo-resist layer;

doping the substrate with ions having the second conductivity type by using the remaining first mask layer as a mask to form a second doped sub-region in the substrate shallower than the first doped sub-region, wherein a doped region having the second conductivity type includes the first doped sub-region and the second doped sub-region;

removing the remaining first mask layer;

partially removing the conductive semiconductor layer to form a gate structure; and

forming a top electrode on the trench structure and the field oxide structure, and forming a bottom electrode on a surface of the substrate opposite to the top electrode;

wherein an ohmic contact is formed between the top electrode and the second conductivity type of the doped region and a Schottky contact is formed between the top electrode and the first conductivity type of the substrate, and a first side of the gate structure is only adjacent to the second conductivity type of the doped region to form the ohmic contact, and a second side of the gate structure is only adjacent to the first conductivity type of the substrate to form the Schottky contact.

2. The method according to claim **1**, further comprising steps of:

forming a mask oxide layer having an opening on the substrate;

doping the substrate with ions having the second conductivity type through the opening to form a guard ring in the substrate; and

partially removing the mask oxide layer to from the field oxide structure.

3. The method according to claim **2** wherein the step of forming the mask oxide layer having the opening comprises steps of:

forming a second patterned photo-resist layer defining the opening on the mask oxide layer;

etching the mask oxide layer to form the opening; and

removing the second patterned photo-resist layer.

4. The method according to claim **1** wherein the substrate comprises a relatively heavily-doped N-type silicon layer and a relatively lightly-doped N-type epitaxial layer.

5. The method according to claim **4** wherein the ions having the second conductivity type are P-type dopants.

6. The method according to claim **5** wherein the P-type dopants are boron ions.

7. The method according to claim **1**, further comprising a rapid thermal annealing step to activate the ions after the ions are doped into the substrate.

8. The method according to claim **1** wherein the step of forming the conductive semiconductor layer comprises steps of:

forming a polysilicon layer by a chemical vapor deposition (CVD) in the trench structured; and

dry-etching the polysilicon layer using the first patterned photo-resist layer as a mask to form the conductive semiconductor layer.

9. The method according to claim **8** wherein the first mask layer is an oxide layer formed by a thermal oxidation of a portion of the polysilicon layer.

10. The method according to claim **1**, further comprising a step of forming a gate oxide layer between the gate structure and the substrate.

11. The method according to claim **1** wherein the top electrode and the bottom electrode are made of one of aluminum and aluminum alloy.

12. The method according to claim **11**, further comprising steps of:

forming an adhesion layer made of one of titanium and titanium nitride between the top electrode and the substrate; and

performing a rapid thermal annealing step to enhance the bonding effect of the adhesion layer.

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